Docket No. 1004378.53100

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Patent No.: 7,443,240 B2

Applicant(s): Hiroshi KATSUNAGA et al.

Issued: October 28, 2008 Customer No.: 85775

For: AM INTERMEDIATE FREQUENCY VARIABLE GAIN AMPLIFIER CIRCUIT, VARIABLE GAIN AMPLIFIER CIRCUIT AND ITS SEMICONDUCTOR INTEGRATED CIRCUIT

**REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached is Form PTO-1050.

☐ The error was the fault of the Patent and Trademark Office, no fee is required.

☒ The error was not the fault of the Patent and Trademark Office, please charge the requisite fee of $100 to Deposit Account No. **504827**, Order No. 1004378.53100.

☒ The Commissioner is hereby authorized to charge any additional fees which may be required by this paper, or credit any overpayment to Deposit Account No. **504827**, Order No. 1004378.53100.

Respectfully submitted,
LOCKE LORD BISSELL & LIDDELL LLP

Dated: July 27, 2009

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**UNITED STATES PATENT AND TRADEMARK OFFICE**
**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,443,240 B2
ISSUED : October 28, 2008
INVENTOR(S): Hiroshi KATSUNAGA et al.
TITLE: AM INTERMEDIATE FREQUENCY VARIABLE GAIN AMPLIFIER CIRCUIT, VARIABLE GAIN AMPLIFIER CIRCUIT AND ITS SEMICONDUCTOR INTEGRATED CIRCUIT

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

**In the Specification**

On Title Page 1, Item (73), please delete "Kabushiki Kaisha Toyota Jidoshokki, Kariya-Shi (JP); Niigata Seimitsu Co., Ltd., Joetsu-Shi (JP)" and insert therefore - - Niigata Seimitsu Co., Ltd., Joetsu-Shi (JP) --;

Column 1, line 45, please delete "referring to FIG. 5(a)-5(c)." and insert therefore - - referring to FIGS. 5(a)-5(c). --;

Column 1, lines 63-64, please delete "resulting in a reduced the drain current Id4" and insert therefore - - resulting in a reduced drain current Id4 --;

Column 2, lines 11-12, please delete "if the input signal level increase" and insert therefore - - if the input signal level increases --;

Column 2, lines 14-15, please delete "When it is considered that the current source 11 of the variable gain amplifier circuit 10" and insert therefore - - The current source 11 of the variable gain amplifier circuit 10 --;

Column 2, lines 40-41, please delete "if a control voltage applied to the gate of a p-channel MOS transistor 25," and insert therefore - - if a control voltage is applied to the gate of a p-channel MOS transistor 25, --;

Column 3, lines 14-15, please delete "for controlling the differential amplification gain of the first and second field-effect transistors, and a bias" and insert therefore - - for controlling the differential amplification gain of the first and second field-effect transistors is applied, and a bias --;

Column 4, line 51, please delete "variable gain amplifier circuit;" and insert therefore - - variable gain amplifier circuit; and --;

Column 5, line 63, please delete "Since constant current 1s is supplied" and insert therefore - - Since constant current Is is supplied --;

Column 6, line 62, please delete "a current source 44 form a current mirror circuit," and insert therefore - - a current source 44 forming a current mirror circuit, --;

Column 8, lines 27-28, please delete "and the resistor R8, it can also comprise one MOS transistor." and insert therefore - - and the resistor R8, but can also comprise one MOS transistor. --; and

Column 8, lines 33-35, please delete "radio set and is can also be applied to the variable gain amplifier circuit of various circuits." and insert therefore - - radio set, but can also be applied to the variable gain amplifier circuit of various circuits. --.

**In the Claims**

In Claim 3, column 9, lines 9-10, please delete "between a source of the first field-effect transistors" and insert therefore - - between a source of the first field-effect transistor --; and

In Claim 6, column 10, lines 1-3, please delete "a fifth field-effect transistor comprising source connected to a power supply" and insert therefore - - a fifth field-effect transistor comprising a source connected to a power supply --.

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